World Class SystemVerilog & UVM Training

Sunburst Design - Expert Clock Domain Crossing (CDC) & FIFO Design Techniques using SystemVerilog

by Recognized Verilog & SystemVerilog Guru, Cliff Cummings of Sunburst Design, Inc.

Cliff Cummings is the only Verilog & SystemVerilog Trainer who helped develop every IEEE & Accellera Verilog, Verilog Synthesis and SystemVerilog Standard.

1 Day
60% Lecture, 40% Lab
Expert Level

Course Objective

To train engineers in the expert topic of multi-clock, Clock Domain Crossing (CDC) and FIFO design techniques using award winning materials developed by renowned Verilog & SystemVerilog Guru, Cliff Cummings.

Upon completion of this course, students will:

- Understand and write efficient RTL models to address:
    - Metastability & synchronizers - synchronizing 1-bit signals
    - Passing multiple control signals - synchronizing multi-bit signals or busses
    - Efficient design & synthesis partitioning techniques
    - Gate-level simulation and corresponding X-propagation issues
    - Multi-clock FIFO design

Course Overview

Sunburst Design - Expert Clock Domain Crossing & FIFO Design Techniques using SystemVerilog is a 1-day intensive course that focuses on some of the most advanced design techniques using SystemVerilog.

This SystemVerilog training was developed and is frequently updated by the renowned SystemVerilog guru and IEEE SystemVerilog committee member, Cliff Cummings. Cliff has presented at numerous SystemVerilog seminars and training classes world wide, including the 2003-2004 SystemVerilog NOW! Seminars, the 2010 ModelSim SystemVerilog Assertion Based Verification Seminars, and multiple Verification Academy DAC seminars.

This course covers advanced multi-clock design techniques not available anywhere else and not commonly taught at the University level.

For more information, contact:
Cliff Cummings - cliffc@sunburst-design.com - Sunburst Design, Inc. - 801-960-1996

Target Audience

Sunburst Design - Expert Clock Domain Crossing & FIFO Design Techniques using SystemVerilog is intended for design engineers who require advanced multi-clock design knowledge.

Prerequisites (mandatory)

This is a very advanced design techniques class that assumes engineers already have a good working knowledge of the Verilog & SystemVerilog languages.

This course assumes that students have a practical working knowledge of SystemVerilog RTL Design.

Course Customization? - Sunburst Design courses can be customized to include **your** company's coding guidelines or to modify the course for a different audience. Sections can be added or deleted from a course to meet you company's needs.

Classroom Details

Training is generally conducted at your facilities. For maximum effectiveness, we recommend having at least one workstation or PC for every two students, with your preferred SystemVerilog simulator licenses (we often can help acquire the simulator and temporary training licenses).

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Course Syllabus - 1-day Course

Multi-clock Clock Domain Crossing (CDC) & FIFO Design Techniques using SystemVerilog

- Very advanced design techniques from Cliff's award-winning presentations on the efficient implementation of multi-clock CDC & FIFO designs. These materials are not specific to SystemVerilog but solutions are shown using SystemVerilog syntax (advanced techniques that all design engineers should know - the stuff you did not learn in college).

- (1) Metastability & synchronizers - synchronizing 1-bit signals
- (2) Passing multiple control signals - synchronizing multi-bit signals or busses
    a. Consolidation
    b. Controlled synchronization - multicycle path formulations (MCP)
    c. FIFO synchronizer
    d. Gray codes & Gray code counters
- (3) Design partitioning - design & synthesis techniques
    a. Naming conventions
    b. Synthesis scripting & timing analysis issues
- (4) Simulation issues
    a. X-propagation issues
    b. Synopsys command for SDF files
    c. Multi-SDF files
    d. ASIC/FPGA vendor cells and models
    e. Simulation model to expose synchronization problems
- (5) Multi-clock FIFO design - large section on design and FIFO issues
- LAB: MCP controlled synchronization lab
- LAB: 2-clock FIFO lab

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