World Class Verilog & SystemVerilog Training

Sunburst Design - SystemVerilog Fundamentals

by Recognized Verilog & SystemVerilog Guru, Cliff Cummings of Sunburst Design, Inc.

Cliff Cummings is the only Verilog & SystemVerilog Trainer who helped develop every IEEE & Accellera Verilog, Verilog Synthesis and SystemVerilog Standard.

2 Days
70% Lecture, 30% Lab
Advanced Level

Course Objective

Introduce engineers to *world class* SystemVerilog language capabilities using award winning materials developed by renowned Verilog & SystemVerilog Guru, Cliff Cummings

Upon completion of this course, students will understand:

- SystemVerilog-2005 language fundamentals
  - includes new SystemVerilog data types and capabilities
  - includes new SystemVerilog RTL and abstraction capabilities
  - includes use of dynamic types and arrays for behavioral modeling
  - includes inclusion of C-models using the new SystemVerilog DPI
  - includes using SystemVerilog Assertions (SVA) for design and verification

Course Overview

Sunburst Design - SystemVerilog Fundamentals is a 2-day fast-paced intensive course that introduces new SystemVerilog features for design, simulation and synthesis. Efficient and proven coding styles are combined with frequent exercises and insightful labs to demonstrate the capabilities of new SystemVerilog features. You will discover that SystemVerilog capabilities are fully backward compatible with Verilog-2001 designs.

This SystemVerilog training was developed and is frequently updated by the renowned SystemVerilog guru and IEEE SystemVerilog committee member, Cliff Cummings, who has presented at numerous SystemVerilog seminars and training classes world wide, including the 2003-2004 SystemVerilog NOW! Seminars and 2010 ModelSim SystemVerilog Assertion Based Verification Seminars.

For more information, contact:
Cliff Cummings - cliffc@sunburst-design.com - Sunburst Design, Inc. - 503-641-8446

Target Audience

Sunburst Design - SystemVerilog Fundamentals is intended for design & verification engineers who require an introduction to IEEE SystemVerilog-2005 capabilities.

Prerequisites (mandatory)

This course assumes that students have a practical working knowledge of Verilog HDL or have completed Verilog HDL training. Engineers with VHDL synthesis experience and some Verilog exposure will do well in this class. Engineers with no prior HDL training or experience will struggle in this class1.

Classroom Details

Training is generally conducted at customer facilities and is sometimes offered as an open-enrollment training class. For maximum effectiveness, it is recommended to have one workstation or PC for every two students, with your preferred SystemVerilog simulator licenses (we often can help provide the simulator and temporary training licenses).

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Course Syllabus

Day One

SystemVerilog Enhancements & Methodology Overview

- Includes a quick review of SystemVerilog resources available to design & verification engineers.

- Verilog & SystemVerilog Keywords
- SystemVerilog Books & Resources
- SystemVerilog Enhancements Strategy & High-Level Methodology

Data Types & Typedefs

- Includes data types, enumerated types, compilation units, packages, casting and randomization functions.

- Nets & Variables Fundamentals & Guidelines
- Blocking & Nonblocking Assignment Fundamentals & Guidelines

- SystemVerilog data types
- Enhanced literal numbers syntax
- Resolved & Unresolved types
- 4-state & 2-state types
- Typedefs
- Near-Universal types
- SystemVerilog type usage guidelines
- Enumerated types
- Struct data type intro
- Type parameters
- Intro to the SystemVerilog program construct
- $unit & $root
- Compilation units & separate compilation
- Packages & :: (package scope operator)
- SystemVerilog package strategies
- Strings
- Static & dynamic type-casting
- Random number generation: $random -vs- $urandom -vs- $urandom_range
- Simulation command aliases & switch definitions
- LABS: Multiple SystemVerilog types, typedefs, type-casting and logic labs

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SystemVerilog Operators, Loops, Jumps. Intro to Logic-Specific Processes, Enhanced functions & tasks

- New always_type blocks help RTL designers. To help verification engineers understand design constructs, the always_type blocks are briefly introduced in this section. Enhancements to tasks and functions make them more useful and easier to use.

- New SystemVerilog operators
- Enhanced loops & jumping statements
- always_comb / always_latch / always_ff - (1-slide introduction only)
- always @* -vs- always_comb
- SystemVerilog enhancements to tasks & functions
- SystemVerilog priority & unique - modifiers for case- & if-statements
- `timescale directive
- SystemVerilog timeunit & timeprecision

Implicit .* and .name Port Instantiation

- Implicit port connections can reduce top-level ASIC and FPGA coding efforts by more than 70% and simultaneously enforce greater port type checking.

- Verilog-2001 positional & named ports
- SystemVerilog .* implicit ports
- SystemVerilog .name implicit ports
- Implicit port connection rules & comparisons - includes IEEE 1800 latest updates
- Strong port-type checking
- New debugging techniques - automatic expansion of .* ports
- Block-level testbenches with implicit ports
- Advantages & disadvantages
- LABS: implicit port instantiation labs
- LABS (optional) : SystemVerilog random numbers

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Day Two

Nonblocking Assignments, Race Conditions & SystemVerilog Event Scheduling
- SystemVerilog is fully backward compatible with Verilog-2001 (it is also fully race backward compatible!) This section describes in detail how the new SystemVerilog event scheduling works and how it will reduce race conditions between RTL designs and verification suites.

- Verillog-2001 Event Scheduling
- 8 guidelines for RTL coding & nonblocking assignments
- SystemVerilog enhanced scheduling - includes IEEE 1800 latest updates
- Verilog -vs- SystemVerilog race conditions
- Scheduling of new SystemVerilog commands
- * Blocking & Nonblocking Assignment Details
- * Mixed RTL & Gate simulations

Structs, Unions, Packed & Unpacked Arrays
- Packed & unpacked arrays, unions and structs allow greater abstraction and more concise coding. The new dynamic array types facilitate behavioral modeling and assist in the development of verification environments.

- Structs & assignment patterns
- Packed & unpacked arrays
- Array indexing
- Structs & packed structs
- Unions & packed unions
- Dynamic arrays & methods
- foreach loop
- Associative arrays & methods
- Queues & concatenation operations
- Queue methods

Interfaces
- Interfaces are a powerful new form of abstraction and this section details how they work for design and verification. This section also discusses when and when not to use interfaces. Virtual interfaces are described after the introduction of virtual classes and virtual methods on day three.

- Interface usage overview
- Introduction to generic interfaces
- Interfaces -vs- records
- How interfaces work
- 4 requirements for good interface usage
- Interfaces - legal & illegal usage
- Interface constructs
- Interface modports
- Generic interfaces
- LABS: multiple interface and interface-protocol labs

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DPI - Direct Programming Interface - SystemVerilog's C-Language Interface
(Optional section - may be omitted to give more time to other topics and labs)
- The Direct Programming Interface (DPI) can be used to simulate C-code with SystemVerilog code. This section describes how this can be done and how DPI programming differs from PLI programming.

- DPI layers
- function import
- function export
- task export
- Using SystemVerilog simulation timing in a C model
- DPI -vs- PLI example
- No PLI required
- How to compile and simulate C-code with SystemVerilog designs
- SystemVerilog & SystemC
- LAB: SystemVerilog using C-code functions

SVA - SystemVerilog Assertions
- This section details how the SystemVerilog Assertion (SVA) syntax works and how assertions can be used for design and verification. Special macro-techniques are shown to reduce assertion coding effort by up to 80%.

- What is an assertion? / Who should add assertions?
- Assertion benefits - bug detection efficiency
- SystemVerilog assertion types
- SystemVerilog immediate assertions
- SystemVerilog concurrent assertions
- Assert & cover properties & labels
- Properties and assert property
- Overlapping & non-overlapping implications
- Edge testing functions
- Sequences
- Vacuous success
- Property styles
- Reduced assertion coding effort using macros
- Macros with default arguments (SystemVerilog-2009 update)
- Assertion coding style efficiency benchmarks
- SystemVerilog assertion system functions
- Sampled value functions
- Assertion severity tasks
- Assertion and coverage example of an FSM design
- Binding SVA to an existing model
- Bind command details and guidelines
- LABS: SystemVerilog Assertions with synchronous FIFO design

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