



World Class SystemVerilog & UVM Training

Sunburst Design - SystemVerilog Assertions (SVA) Training

by Recognized Verilog & SystemVerilog Guru, Cliff Cummings of Sunburst Design, Inc.

Cliff Cummings is the only Verilog & SystemVerilog Trainer who helped develop every IEEE & Accellera Verilog, Verilog Synthesis and SystemVerilog Standard.

6-Hour Training - *Learn SVA in less than half the time and for less than half the price*

50% Lecture, 50% Lab

Advanced Level

Course Motivation

In recent years Cliff has been called on to conduct SystemVerilog Assertion (SVA) training for companies that had previously taken multi-day SVA training, not because the training they received was bad, but because the training they received was too much and their engineering teams had a hard time remembering all of the SVA options and syntax possibilities. The problem is that engineers use SVA sporadically for a few months on one project, then they might go many months before they need to use it again.

Course Objective

Learn concise, syntax error-avoidance coding styles to make design and verification engineers productive and make them eager to use assertions in RTL designs. Experience has shown that engineers can become efficient after 2-3 hours of SVA lecture and 2-3 hours of SVA lab work. In this course, engineers will be trained to:

- Use ***bindfiles*** to add assertions to a design
- Use long, descriptive labels to:
 - document the assertions
 - accelerate debugging using waveform displays
- Use simple macros to:
 - efficiently add concise assertions
 - reduce assertion coding efforts
 - reduce assertion syntax errors
- Use concurrent assertions but avoid immediate assertions
- Use `|-> ##1` implications instead of `|=>` implications
- Gain valuable SVA writing and debugging experience through lab work where engineers are asked to debug a 1-clock synchronous FIFO design with 8 subtle bugs.

These recommendations, and more, are taught in this class and described in the award-winning paper, *SystemVerilog Assertions - Bindfiles and Best Known Practices for Simple SVA Usage*:

www.sunburst-design.com/papers/CummingsSNUG2016SV_SVA_Best_Practices.pdf

For more information, contact:

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Unless an engineer has a fulltime job adding assertions to all of the projects at a company, engineers should focus on a concise and efficient subset of the SVA syntax and capabilities and augment their assertion checking with additional SVA capabilities as needed.

Course Overview

Sunburst Design - SystemVerilog Assertions (SVA) Training is a ~6-hour hands-on course that focuses on simple, efficient and proven SVA features for design and verification. Efficient and proven coding styles are combined with an insightful FIFO-debug lab to demonstrate assertion creation and debugging capabilities.

This SVA training was developed and is frequently updated by the renowned SystemVerilog guru and IEEE SystemVerilog committee member, Cliff Cummings. Cliff has presented at numerous SystemVerilog seminars and training classes world wide, including the 2003-2004 SystemVerilog NOW! Seminars, the 2010 ModelSim SystemVerilog Assertion Based Verification Seminars, and multiple Verification Academy DAC seminars.

Target Audience

Sunburst Design - SystemVerilog Assertions (SVA) Training is intended for design and verification engineers who require efficient and productive SVA knowledge to help rapidly identify and correct design bugs.

Prerequisites (mandatory)

This is an advanced SystemVerilog class that assumes engineers already have a good working knowledge of the SystemVerilog language.

The Sunburst Design - Advantage

Who is teaching your "expert" and "advanced" classes? Most companies will not tell you because their instructors might not have much design experience or may never have participated on any of the Verilog or SystemVerilog Standards groups or presented at industry recognized conferences. Go to our web site and read about the Sunburst Design - Instructors - they are the best and they have the experience and qualifications to offer best-in-class training.

Classroom Details

Training is generally conducted at your facilities. For maximum effectiveness, we recommend having at least one workstation or PC for every two students, with your preferred SystemVerilog simulator licenses (we often can help acquire the simulator and temporary training licenses).

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Course Syllabus

SVA - SystemVerilog Assertions

- This training details how the SystemVerilog Assertion (SVA) syntax works and how assertions can be used for design and verification. Special macro-techniques are shown to reduce assertion coding effort by up to 80%.

- What is an assertion? / Who should add assertions?
- Assertion benefits - bug detection efficiency
- SystemVerilog assertion types
- SystemVerilog immediate assertions
- SystemVerilog concurrent assertions
- Assert & cover properties & labels
- Properties and assert property
- Overlapping & non-overlapping implications
- Edge testing functions
- Sequences
- Vacuous success
- Property styles
- Reduced assertion coding effort using macros
- Macros with default arguments (SystemVerilog-2009 update)
- Assertion coding style efficiency benchmarks
- SystemVerilog assertion system functions
- Sampled value functions
- Assertion severity tasks
- Assertion and coverage example of an FSM design
- Binding SVA to an existing model
- Bind command details and guidelines
- LAB: SystemVerilog Assertions with synchronous FIFO design

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